Nayyan Mujadiya

Nayyan's Resumé

One should apply knowledge for the benefit of our industry and people - JRD Tata

Career objective

Aim To become a successful professional in the field of technology and to work for the best, strive for excellence and learn continuously in the process, in an innovative and competitive world.

Experience

Professional

Aug 2022 – Present **Lead Member Consulting Staff**, *Siemens EDA India Pvt. Ltd.*, Bengaluru.
worked on Global Analysis engine of Questa Tool chain.

Nov 2021 – Aug 2022 **R&D Engineer Staff**, *Synopsys India Pvt. Ltd.*, Bengaluru.
worked on making Design Compiler NXT thread-Safe.

June 2018 – Oct 2021 **R&D Engineer Sr II**, *Synopsys India Pvt. Ltd.*, Bengaluru.
worked on Common physical library and block abstract models with IC Compiler II, while retaining support for the Milkyway^{TM} library format

June 2014 – May 2018 **R&D Engineer Sr I**, *Synopsys India Pvt. Ltd.*, Bengaluru.
Experience in EDA tool development. Worked on Logic Synthesis - mainly DRC fixing, QoR improvement, run-time improvement & Scan-Chain Optimization.

Dec 2012 – May 2014 **R&D Engineer II**, *Synopsys India Pvt. Ltd.*, Bengaluru.
I worked on the development of Design Compiler (developed in C) - a synthesis tool. The work involves improving run-time of DRC fixing engine. I was able to improve run-time *1%* by optimizing 'sot-sdn' - a sizing engine. I implemented - 'caching mechanism' - storing the move and skipping if earlier it was failed. I also worked on 'report_congestion' command. Also fixed several critical bug to make product more stable.

Feb 2011 – Dec 2012 **Software Engineer I**, *Microsemi India Pvt. Ltd.*, Hyderabad.

Jan 2011 – Jan 2011 **Software Intern**, *Actel India Pvt. Ltd.*, Hyderabad.
I worked on the development of multi-tier application for generating optimum hardware using C++, STL, some Boost Libraries, Qt and Tcl. The work involves designing custom UI in Qt, i.e. the front end, developing the middleware (primarily Tcl + Actel custom engine) and the actual backend involving C++, STL and Boost. Also worked on writing HDL from internal netlist format (SmartDesign to HDL). I have experience in interacting with teams in distributed locations.

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Aug 2009 – July 2010 **R&D Intern**, *Synopsys India Pvt. Ltd.*, Bengaluru.
I worked on "Balanced-Buffer tree" and other optimization techniques for Design CompilerTool along with regular maintenance work. Design Compiler is Synthesis tool which takes HDL programs as input and generates gate-level hardware as output. I have primarily used C, several internal libraries, Tcl and Perl.

Academic

Dec 2004 – Apr 2005 **Research Trainee**, *Space Application Center, ISRO*, Ahmedabad.

Publications

- Nayan V. Mujadiya, **"Instruction Scheduling for VLIW Processors Under Variation Scenario"**, IEEE International Conference on Embedded Computer Systems: Architectures, Modeling, and Simulation (IC-SAMOS), June 2009.
- Nayan V. Mujadiya, **"Instruction Scheduling on Variable Latency Functional Units of VLIW Processors"** in ISED '11: Accepted for International Symposium on Electronic System Design 2011.

Master's thesis

Title **Instruction Scheduling for VLIW Processors under Variation Scenario**

Supervisors Dr. Madhu Mutyam

Description Due to process variation, components like adders, multipliers, etc., of different Integer FUs in VLIW processors may operate at various speeds, resulting in non-uniform latency IFUs which can cause performance loss. We have presented three compile-time techniques namely 'turn-off', 'on-demand turn-on' and 'mobility-list-scheduling' to handle these non-uniform latency IFUs and reduces the power-performance penalty.

Education

2007–2011 **MS by Research**, *International Institute of Information Technology*, Hyderabad, *7.4 CPGA*.
Computer Architecture and Compiler Optimization

2006–2007 **M.Tech**, *International Institute of Information Technology*, Hyderabad, *7.4 CGPA*.
CSE

2001–2005 **B.E.**, *Dharmsinh Desai Institute of Technology*, Nadiad, *63%*.
Information Technology

2000–2001 **Class 12**, *L.M.P. Reva Exp.*, Bilimora, *83.5%*.
Science

1998–1999 **Class 10**, *L.M.P. Reva Exp.*, Bilimora, *82%*.
Maths

Other Areas of Interest

- High Performance Computing
- FPGA
- Computer Architecture
- IoT
- Compiler Optimization
- Embedded System
- Parallel Algorithms
- Computational Geometry

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Technick skills

- Programming Language :- **C, C++ with STL and boost, Python, Java basics**
- Scripting Languages :- **Perl, Tcl, Rubby, C Shell Scripting**
- HDL :- **Verilog, VHDL**

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